ELECTRICAL CONDUCTING STRUCTURE AND LIQUID CRYSTAL DISPLAY DEVICE COMPRISING THE SAME

DESCRIPTION

Background of Invention

[Para 1] 1. Field of the Invention

[Para 2] The invention relates to a conducting structure, and more particularly, to a conducting structure with flexibility.

[Para 3] 2. Description of the Prior Art

[Para 4] In the fabrication of liquid crystal displays, some of the module package techniques common used today includes tape automated bonding (TAB), chip on glass (COG), and chip on film (COF). In TAB, numerous bumps are utilized for connecting a polyimide board and a liquid crystal display panel via an anisotropic conductive film (ACF) after the driving chip is fabricated. The bumps are essentially metal blocks comprising gold or lead-tin alloy on the bonding pad of the chip and during fabrication, the bumps are melted to connect the bonding pad and the circuits together. In COG, driving chips with fabricated bumps are connected directly onto an LCD panel by an anisotropic conductive film via a flip chip package. In COF, the electrical circuit originally designed for the printed circuit board is positioned on the polyimide board together with the driving chip.

[Para 5] In the past, TAB has generally been utilized for fabricating larger LCD panels whereas COG has been used for fabricating medium to small size LCD panels. However in recent years, COG has been widely used for fabricating LCD panels of various sizes in order to reduce cost of the panels.

Nevertheless, numerous problems that ultimately affect production yield and quality of display still remain when the existing COG technique is applied to LCD panel fabrication.

[Para 6] Please refer to Fig. 1. Fig. 1 is a schematic view of the COG technique according to the prior art. By fabricating bumps 106 on the pad of an integrated circuit 102 and utilizing an anisotropic conductive film 108 as the interface, the integrated circuit 102 can be smoothly connected onto an LCD panel 104. In general, the bumps 106 are composed of materials such as gold or lead-tin alloy and the anisotropic conductive film 108 is composed of materials including numerous conductive pellets. By melting the conductive pellets between the bumps 106 and the anisotropic conductive film 108 via a hot embossing fabrication, the integrated circuit 102 can be electrically connected to a connection pad on the LCD panel 104. A high temperature (160 to 190°C) is normally required to carry out the hot embossing fabrication, and because of the fact that the heat expansion coefficient between the integrated circuit 102 and the LCD panel 104 differs significantly, an enormous amount of stress is often generated at the contact surface when the temperature returns to normal. As shown in Fig. 2, the resulting stress often causes a bending phenomenon on the integrated circuit 102 and the LCD panel 104. Eventually, the phenomenon would further induce a curtain mura and degrade the overall quality of the display.

[Para 7] In the prior art COG technique, the smoothness of the LCD panel 104 becomes particularly important as the integrated circuit 102 and the LCD panel 104 are composed of hard and rigid materials. In general, the smoothness of the LCD panels must be controlled to within a range of $\pm 0.5\,\mu$m and the smoothness requirements for larger LCD panels are even stricter. Essentially, an LCD panel with poor smoothness often results in a connection failure between the integrated circuit 102 and the LCD panel 104 and ultimately decreases the overall product yield.

[Para 8] Moreover, since the anisotropic conductive film that includes numerous conductive pellets is commonly used for connecting the integrated circuit 102 and the LCD panel 104, maintaining a safe distance between the bumps 106 therefore becomes a critically important matter for preventing a short circuit. Please refer to Fig. 3. Fig. 3 is a schematic view of the connection between the bump 106, conductive pellets 108a, and the integrated circuit 102 and LCD panel 104. If the distance between the bumps 106 is too short and the conductive pellets 108a are concentrated in one area, a short circuit will be occurred between the bumps 106 and it will decrease the product yield. According to the prior art about COG technique, a distance of more than 15 μm between the bumps 106 is generally required in order to control the probability of a short circuit to be within an acceptable range. As a result, the contact area between the integrated circuit and the LCD panel needs to be maintained above a certain size and it is an unavoidable challenge to reducing the size of the contact area.

Summary of Invention

[Para 9] It is therefore an objective of the present invention to provide a conductive structure with flexible bumps for effectively preventing the bending phenomenon between the integrated circuit and the LCD panel and problems such as curtain mura.

[Para 10] In addition, a second objective of the present invention is to provide a conductive structure with flexible bumps for increasing the tolerance level of Chip On Glass (COG) technique to the smoothness of the glass substrate.

[Para 11] The third objective of the present invention is to provide a conductive structure with bumps surrounded by an insulating layer for preventing short circuits and for reducing the contact area between the integrated circuit and the LCD panel.

[Para 12] According to the present invention, a conductive structure includes an integrated circuit, a substrate, and a plurality of bumps located between the integrated circuit and the substrate. At least one bump comprises a first conductive part connected to the integrated circuit at one end; a second conductive part connected to the integrated circuit at one end; a conductive connection part connecting the first conductive part and the second conductive part; a first insulation part surrounding the first conductive part and the second conductive part; and a second insulation part locating between the first conductive part and the second conductive part.

[Para 13] According to the present invention, a liquid crystal display comprises a substrate, a liquid crystal display region positioned in the center of the substrate, an integrated circuit positioned on the edge of the substrate, a plurality of bumps positioned between the substrate and the integrated circuit for electrically connecting the integrated circuit, and an anisotropic conductive film for providing an electrical connection between the bumps and the substrate. At least one bump comprises a first conductive part connected to the integrated circuit at one end; a second conductive part connected to the integrated circuit at one end; a conductive connection part connecting the first conductive part and the second conductive part; a first insulation part surrounding the first conductive part and the second conductive part; and a second insulation part locating between the first conductive part and the second conductive part.

[Para 14] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[Para 15] Fig. 1 is a schematic view of the COG technique according to the prior art.

[Para 16] Fig. 2 is a schematic view of the bending phenomenon caused by the COG technique according to the prior art.

[Para 17] Fig. 3 is a schematic view of a short circuit condition caused by the COG technique according to the prior art.

[Para 18] Fig. 4 is a schematic view of the means by which the bumps of the conductive structure are connected to the integrated circuit according to the present invention.

[Para 19] Fig. 5 is a schematic view of the means by which the bumps of the conductive structure are connected to the integrated circuit according to the present invention.

[Para 20] Fig. 6 is a schematic view of the conductive structure in which the bumps are connected to the integrated circuit and the glass substrate according to the present invention.

[Para 21] Fig. 7 is a schematic view of the conductive structure in which the bumps are connected to an uneven surface according to the present invention.

[Para 22] Fig. 8 is a schematic view of the conductive structure in which the distance between bumps is reduced according to the present invention.

[Para 23] Figs. 9, 10, and 11 show schematic upward views of the bumps of the conductive structure according to the present invention.

[Para 24] Figs. 12 and 13 show another embodiment of the bumps of the conductive structure according to the present invention.

[Para 25] Figs. 14 and 15 show another embodiment of the bumps of the conductive structure according to the present invention.

[Para 26] Figs. 16 and 17 show another embodiment of the bumps of the conductive structure according to the present invention.

Detailed Description

[Para 27] Please refer to Fig. 4 and Fig. 5. Fig. 4 and Fig. 5 are schematic views of the means by which the bumps of the conductive structure are connected to the integrated circuit according to the present invention. The bumps in Fig. 4 and Fig. 5 comprise a first conducting part 2041, a second conducting part 2042, a conductive connection part 208, and an insulation layer 206. The insulation layer 206 can be further divided into a first insulation part 2101 and a second insulation part 2102 based on its location of formation. One end of the first conductive part 2041 and one end of the second conductive part 2042 are connected to the integrated circuit 202, and the other ends of the two conductive parts are connected to the conductive connection part 208. The first conductive part 2041 and the second conductive part 2042 are surrounded by the first insulation part 2101. The second insulation part 2102 is located between the first conductive part 2041 and the second conductive part 2042.

[Para 28] During the fabrication of the conductive structure bumps, the insulation layer 206 is first formed on a contact of the integrated circuit 202 and two openings are formed on the insulation layer 206 to expose the contact of the integrated circuit 202. Then a first conductive part 2041 and a second conductive part 2042 are formed in the two openings. Thereafter, a conductive connection part 208 is formed on the first conductive part 2041 and the second conductive part 2042. The conductive connection part 208 is electrically connected to the integrated circuit 202 through the first conductive part 2041 and the second conductive part 2042. The insulation layer 206 is divided into the first insulation part 2101 and the second insulation part 2102. The first insulation part 2101 surrounds the first conductive part 2041 and the second conductive part 2042, whereas the second insulation part 2102 is located between the first conductive part 2041 and the second conductive part 2042. The insulation layer 206 comprises light-isolating materials such as polyimide (PI), a strong isolating material with flexibility. In order to form the first conductive part 2041 and the second conductive part 2042, an electroless fabrication method can be employed to form gold, nickel, gold alloy, or nickel alloy in the openings, and ultimately to electrically connect to the contact of the integrated circuit 202. In addition, the composition of the conductive connection part 208 is selected from materials such as gold or gold alloys.

[Para 29] In the preferred embodiment of the present invention, when the height of the first conductive part 2041 and the second conductive part 2042 is H1, the height of the conductive connection part 208 is H2, and the height of the first insulation part 2101 is H3, the relationship among the three heights becomes $H1 \leqq H3 \leqq H1+H2$. The condition where $H1=H3$ is shown in Fig. 4, while the condition where $H3=H1+H2$ is shown in Fig. 5.

[Para 30] Please refer to Fig. 6. Fig. 6 is a schematic view of the conductive structure in which the bumps are connected to the integrated circuit and the glass substrate according to the present invention. In order to establish a connection between the integrated circuit 202 and the glass substrate 212, the

integrated circuit 202 needs to be electrically connected to a contact pad on top of the glass substrate 212 via hot embossing fabrication by melting the conductive connection part 208 and the conductive pellets 210. After the integrated circuit 202 and the glass substrate 212 return to room temperature, the stress remaining in the contact surface is removed by a deformation of the bumps due to their flexible nature. As shown in Fig. 6, the bump is deformed into a trapezoid structure to remove the stress remaining in the horizontal direction. Consequently, the bending phenomenon of the integrated circuit 202 and the glass substrate 212 is greatly reduced and problems such as curtain mura can also be prevented.

[Para 31] Please refer to Fig. 7. Fig. 7 is a schematic view of the conductive structure in which the bumps are connected to an uneven surface according to the present invention. The condition shown in Fig. 7 during the compression process is often caused by an uneven surface on the integrated circuit 202 and/or the glass substrate 212. Due to the compressible nature of the bumps and the fact that the insulation layer 206 is composed of a flexible material, the bumps are able to conform with the compression surface to a certain extent. By utilizing the bumps of the present invention, a greater tolerance level to the smoothness of the LCD panel is achieved and thus, the overall fabrication yield is increased.

[Para 32] Please refer to Fig. 8. Fig. 8 is a schematic view of the conductive structure in which the distance between bumps is reduced according to the present invention. Even when the distance between the bumps is reduced and the conductive pellets 210 are concentrated between two bumps, the bumps are still electrically insulated from each other due to the design of the insulation layer 206. As a result, the area of the contact region and the distance between the integrated circuit 202 and the glass substrate 212 can be greatly reduced. As shown in Fig. 8, the insulation layer 206 only separates the contact between the first conductive part 2041 and the second conductive part 2042 but not the neighboring conductive connection part 208. In another

preferred embodiment, the insulation layer 206 can be extended downward to further protect the conductive connection part 208, as shown in Fig. 5.

[Para 33] Please refer to Fig. 9. Fig. 9 is a schematic upward view of the bumps of the conductive structure according to the present invention. As shown in Fig. 9, the upward view of both the first conductive part 2041 and the second conductive part 2042 is rectangular. The shape of these two conductive parts can also be square, as shown in Fig. 10 or circular, as shown in Fig. 11. Essentially, a bump should include at least one conductive part, such as the two conductive parts 2041 and 2042 as shown in Fig. 9, or a plurality of conductive parts 2041 and 2042, as shown in Fig. 10 and Fig. 11. As long as the conductive connection part 208 is electrically connected to the contact of the integrated circuit 202, the first conductive part 2041 and the second conductive part 2042 can be triangular, tetragonal, polygonal, cylindrical, or elliptical.

[Para 34] Please refer to Fig. 12 and 13. Fig. 12 and Fig. 13 show another embodiment of the bumps of the conductive structure according to the present invention. As shown in Fig. 12, the first conductive part 2041 and the second conductive part 2042 are a monolithically-formed structure. The structure has a hollow region in the center. The second insulation part 2102 is located within the hollow region, and the first conductive part 2041 and the second conductive part 2042 are surrounded by the first insulation part 2101. As shown in Fig. 13, a plurality of the first conductive part 2041 and the second conductive part 2042 comprising the hollow region in the center are utilized for forming the bumps of the present invention. In Fig. 13, the second insulation part 2102 is also located within the hollow region and the first conductive part 2041 and the second conductive part 2042 are surrounded by the first insulation part 2101.

[Para 35] Please refer to Fig. 14 and Fig. 15. Fig. 14 and Fig. 15 show another embodiment of the bumps of the conductive structure according to the present invention. As shown in Fig. 14, the first conductive part 2041 and the second conductive part 2042 are a monolithically-formed structure. The structure has a square hollow region in the center. The second insulation part 2102 is located within the hollow region, and the first conductive part 2041 and the second conductive part 2042 are surrounded by the first insulation part 2101. As shown in Fig. 15, a plurality of the first conductive part 2041 and the second conductive part 2042 comprising the square hollow region are utilized for forming the bumps of the present invention. In Fig. 15, the second insulation part 2102 is also located within the square hollow region and the first conductive part 2041 and the second conductive part 2042 are surrounded by the first insulation part 2101. In this embodiment, the first conductive part 2041 and the second conductive part 2042 neighboring to each other can be interconnected to form an even stronger structure.

[Para 36] Please refer to Fig. 16 and Fig. 17. Fig. 16 and Fig. 17 show another embodiment of the bumps of the conductive structure according to the present invention. This embodiment is essentially a variation derived from the embodiment shown in Fig. 12 and Fig. 13. As shown in Fig. 16, the first conductive part 2041 and the second conductive part 2042 are a monolithically-formed structure. The first conductive part 2041 and the second conductive part 2042 also form a hollow post that includes an opening. The external first insulation part 2101 and the internal second insulation part 2102 form a monolithically-formed structure that eventually becomes the insulation layer 206. As shown in Fig. 17, a plurality of the first conductive part 2041 and the second conductive part 2042 comprising the hollow post are utilized for forming the bumps of the present invention.

[Para 37] Since the integrated circuit 202 and the glass substrate 212 are composed of hard and rigid materials, a modified conductive bump can be further utilized according to the present invention to increase the tolerance

level of the COG technique to the smoothness of the glass substrate. The modified conductive bump includes a buffer layer that is capable of undergoing deformation during a connection. The buffer layer deformation is able to compensate for connection problems caused by uneven contact between the bumps and the glass substrate and the height of the bumps, and consequently increases fabrication variability and production yield. In addition, a multi-layered metal layer is formed on top of the buffer layer. The multi-layered metal layer is composed of an adhesion layer, a shielding layer, and a protective layer and the conductive bump is positioned on top of the metal layer. Characterized by having a buffer layer with low Young's modulus, the conductive bump ensures a much tighter connection during an affixing process and also prevents having uneven electrical resistance at the point of contact.

[Para 38] In contrast to the prior art, the present invention introduces the conductive structure to provide distinguishing features including bendable and compressible bumps that are insulated from each other horizontally, thereby effectively reducing the production cost, reducing the final product size, and increasing the product yield.

[Para 39] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.